

## **Senior Process Integration Engineer**

### **Job Description:**

Well funded start-up company with advanced non-volatile (spin-transfer torque) STT-RAM technology seeking semiconductor CMOS and memory integration engineer for transistor device and memory product development.

### **Responsibilities:**

- Responsible for process development and process integration for advanced (90 nm, 65 nm, 45 nm) CMOS technology with main focus on memory device fabrication. Initiate the process specification and design process flow to meet the device performance.
- Responsible for parametric test structure design and associated mask layout. Involved in device test and characterization as well as data extraction.
- Propose design of experiments (DOE).
- Interface with foundry for process qualification and implementation.
- Establish entitlement yield capability on STT-RAM technology.
- Support the analysis and debug of STT-RAM memory test results.
- Some travel is required in this position.

### **Required Skills:**

- Hands-on experience in semiconductor CMOS and memory process technology. Strong background in semiconductor transistor physics.
- Experience with statistic data analysis tools.
- Working knowledge in mask layout tools and TCAD tools for both process and device simulation.
- Knowledge in semiconductor bench test systems and device characterization techniques.
- Self-motivated, good teamwork skills, ability to multi-task, work and communicate effectively in fast paced environment.

### **Required Experience:**

Extensive experience (> 5 years) in CMOS device and memory product fabrication and integration in major semiconductor companies is preferred.

### **Required Education:**

BS, MS, or Ph.D. in Electrical Engineering, Chemical Engineering, Mechanical Engineering, or Physics.

### **Compensation:**

We offer a very competitive compensation package that includes a stock option plan and a patent bonus program. Employees also receive medical, dental, vision and life insurance fully paid by the company, as well as a 401K plan. This position is located in Milpitas (Silicon Valley), California.